UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,101	07/08/2003	Michael A. Filippo	5500-89400	8643

53806 7590 05/18/2007

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL (AMD)
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
05/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,101	FILIPPO ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are pending.

Papers Filed

Examiner acknowledges receipt of amendments and remarks filed 28 February 2007.

Claim Rejections - 35 USC § 112

1. Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The amendments to each of the independent claims requires that the index be "fixed". Applicant's remarks have given some insight on the meaning of this term; however, according to Applicant an index value derived from an address is variable. Moreover, Paragraph 47 of Applicant's specification shows that Applicant uses this exact technique for generating an address. Therefore, it appears that Applicant has amendment beyond the support of the specification.

Rather than reject the claim for failing to satisfy the enablement requirement, Examiner has chosen to simply view the word "fixed" as indefinite.

Claim Rejections - 35 USC § 103

Hughes and Webb fail to disclose reissuing instructions that result in incorrect output and instructions dependant on those instructions.

Examiner asserts it is common in the art to reissue these types of instructions when the output is not a desired result.

Hughes and Web would have been motivated to utilize this technique because reissuing instructions is a common, simple, fast, and effective technique for gaining the correct output. In fact, Examiner is not aware of any other technique.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of either Hughes and Web and combine it with the ability to reissue instructions when the original output is not a desired result.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – .
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 8-10, 13-16, 18, 20-22, 24, 27, 28, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Hughes (International Application WO 01/35212) which was cited on Applicant's information disclosure statement filed 27 February 2006.

4. As per claims 1 and 14, Hughes discloses a microprocessor and computer system, comprising: a dispatch unit configured to dispatch load and store operations (page 12 lines 6-12);

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb in view of common.

Webb inherently requires the use of a STLF checker configured to verify the operation of the STLF buffer.

However, even if this inherency were not true, it is further obvious to use a STLF checker to verify the operation of the STLF buffer.

Examiner takes Official Notice that accurate storing of information is typically required for accurate output. Examiner further asserts that errors can occur based on hazards, soft errors, etc.

Therefore, it would have been obvious at the time of the invention for one of ordinary skill in the art to take the processor of Webb and allow for a STLF checker to verify correct operation on the STLF buffer.

1. Claims 11, 12, 19, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb in view of common art and Hughes in view of common art.

Hughes and Web disclose the microprocessor of claim 9 and the method of claim 28.

and a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit (Fig. 1), wherein the load store unit includes an indexed STLF (Store-to-Load Forwarding) buffer (Fig. 1), wherein the indexed STLF buffer includes a plurality of entries (Fig. 1 and page 15 lines 24-28); wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to index into the indexed STLF buffer using the general index to select one of the plurality of entries, and to forward data included in the one of the plurality of entries as a result of the load operation. (page 34 lines 21-30 and claims 1-2)

5. As per claims 2 and 15, Hughes discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit is configured to not forward the data included in the one of the plurality of entries as the result of the load operation if information included in the one of the plurality of entries does not match information associated with the load operation. (page 34 lines 21-30 and claims 1-2) *The examiner asserts that if the address does not match, an entry is not forwarded on a data load operation.*

6. As per claims 3 and 22, Hughes discloses the microprocessor of claim 1 and the method of claim 20, wherein the one of the plurality of entries in the STLF buffer is configured to store an address, data, and a data size (Fig. 1) associated with a store operation.

7. As per claims 5, 16 and 24, Hughes discloses the microprocessor of claim 1, computer system of claim 14 and the method of claim 20, wherein the load store unit is configured to

select which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion of an address of the store operation. (Fig 1 ADDR - Tag)

8. As per claims 8 and 27, Hughes discloses the microprocessor of claim 5 and the method of claim 24, wherein the additional index comprises a portion of the address targeted by the store operation. (Fig 1 ADDR - Tag)

9. As per claims 9 and 18, Hughes discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer. (Fig. 1 Hit control Circuit 402 and page 2 lines 28-32)

10. As per claims 10 and 28, Hughes discloses the microprocessor of claim 9 and the method of claim 20, wherein the STLF checker is configured to perform an associative address comparison to identify all issued store operations targeting a same address as the load operation and to implement a find-first algorithm to select a youngest issued store operation that is older than the load operation. (Page 8 lines 14-17)

11. As per claims 13 and 31, Hughes teaches the microprocessor of claim 9, wherein the load store unit is configured to identify the result of the load operation as a speculative value in response to forwarding the data in the one of the plurality of entries included in the STLF buffer as the result of the load operation; wherein if the STLF checker verifies that the STLF buffer

operated correctly for the load operation, the load store unit is configured to indicate that the result of the load operation is not speculative. (abstract and claims 1-4)

12. As per claim 20, Hughes discloses a method, comprising: receiving an address of a load operation; generating an index corresponding to the address; using the index to select an entry from a plurality of entries included in a STLF (Store-to-Load Forwarding) buffer; and forwarding data included the entry as a result of the load operation. (abstract, Fig. 1 and page 15 lines 24-28)

13. As per claim 21, Hughes discloses the method of claim 20, wherein said forwarding is dependent on information included in the entry matching information associated with the load operation. *The examiner asserts that the forwarding of an entry is dependant on the physical address matching.*

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 4 and 23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes.

16. As per claims 4 and 23, Hughes discloses the microprocessor of claim 1 and the method of claim 20, but fails to disclose each of the plurality of entries in the STLF buffer has a capacity

to store a maximum amount of data that can be written by a store operation. Hughes does not disclose the data bus width of the processor of his invention.

17. Official Notice is taken that data buses of sizes 8, 16, 32 or 64-bit are extremely well known in the art. With any of these data buses in place in Hughes' invention, the data buffer would be able to hold at least the maximum amount of data specified by a data store operation.

18. A data bus having a given size less than or equal to 64 bits is beneficial in a processor in that costs of implementation are limited. Larger data buses require processor components to also grow in size, increasing processor area, power consumption and cost.

19. Implementing a data bus less than or equal to 64 bits in Hughes' invention would have been obvious at the time of invention to one of ordinary skill in the art for the benefit of limiting costs, size and power consumption.

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

21. Claims 1-3, 5, 8-10, 14-16, 18, 20-22, 24, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Webb et al. (U.S. Patent No. 6,360,314) hereinafter referred to as Webb.

22. As per claims 1 and 14, Webb discloses a microprocessor and computer system, comprising: a dispatch unit configured to dispatch load and store operations (Fi.g 1 clock cycle:

Issue) *The examiner asserts that a unit is responsible for issuing operations*; and a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit (Fig. 4), wherein the load store unit includes an indexed STLF (Store-to-Load Forwarding) buffer (Fig. 4 buffer 428 and queue 426), wherein the indexed STLF buffer includes a plurality of entries (Fig. 7); wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to index into the indexed STLF buffer using the general index to select one of the plurality of entries (Col. 5 lines 5-8 and 19-22), and to forward data included in the one of the plurality of entries as a result of the load operation. (Col. 2 lines 8-15)

23. As per claims 2 and 15, Webb discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit is configured to not forward the data included in the one of the plurality of entries as the result of the load operation if information included in the one of the plurality of entries does not match information associated with the load operation. (Col. 2 lines 7-15) *The examiner asserts that if the address does not match, an entry is not forwarded on a data load operation.*

24. As per claims 3 and 22, Webb discloses the microprocessor of claim 1 and the method of claim 20, wherein the one of the plurality of entries in the STLF buffer (Fig. 7) is configured to store an address (Fig. 7 address 42), data (Fig. 7 word 52), and a data size (Fig. 7 size 48) associated with a store operation.

25. As per claims 5, 16 and 24, Webb discloses the microprocessor of claim 1, computer system of claim 14 and the method of claim 20, wherein the load store unit is configured to select which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion of an address of the store operation. (Col. 5 lines 5-8 and 19-23)

26. As per claims 8 and 27, Webb discloses the microprocessor of claim 5 and the method of claim 24, wherein the additional index comprises a portion of the address targeted by the store operation. (Col. 5 lines 19-22)

27. As per claims 9 and 18, Webb discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer. *The examiner asserts that Webb's invention contains a unit which verifies operation, specified as the apparatus disclosed in col. 7, lines 5-8.*

28. As per claims 10 and 28, Webb discloses the microprocessor of claim 9 and the method of claim 20, wherein the STLF checker is configured to perform an associative address comparison to identify all issued store operations targeting a same address as the load operation and to implement a find-first algorithm to select a youngest issued store operation that is older than the load operation. (Col. 7 lines 3-36)

29. As per claim 20, Webb discloses a method, comprising: receiving an address of a load operation; generating an index corresponding to the address; using the index to select an entry from a plurality of entries included in a STLF (Store-to-Load Forwarding) buffer; and forwarding data included the entry as a result of the load operation. (Col. 5 lines 5-22)

30. As per claim 21, Webb discloses the method of claim 20, wherein said forwarding is dependent on information included in the entry matching information associated with the load operation. *The examiner asserts that the forwarding of an entry is dependant on the physical address matching.*

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claims 4 and 23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb.

33. As per claims 4 and 23, Webb discloses the microprocessor of claim 1 and the method of claim 20, but fails to disclose each of the plurality of entries in the STLF buffer has a capacity to store a maximum amount of data that can be written by a store operation. Webb further discloses the data entry to hold any of a quadword, longword, word or byte (Col. 4 line 66-67) but does not disclose the data bus width of the processor of his invention.

34. Official Notice is taken that data buses of sizes 8, 16, 32 or 64-bit are extremely well known in the art. With any of these data buses in place in Webb's invention, the data buffer would be able to hold at least the maximum amount of data specified by a data store operation.

35. A data bus having a given size less than or equal to 64 bits is beneficial in a processor in that costs of implementation are limited. Larger data buses require processor components to also grow in size, increasing processor area, power consumption and cost.

36. Implementing a data bus less than or equal to 64 bits in Webb's invention would have been obvious at the time of invention to one of ordinary skill in the art for the benefit of limiting costs, size and power consumption.

Allowable Subject Matter

2. Claim 6, 7, 17, 25, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and the 35 U.S.C. 112 rejection has been satisfied.

Response to Arguments

3. Applicant's arguments filed 28 February 2007 have been fully considered but they are not persuasive.

1. Applicant states:

Regarding claim 12, Applicant argues that it is not inherent to reissue dependent instructions. Applicant states that dependent instructions can be prevented from being issued until independent instructions have completed.

Examiner admits that this is an alternative would prevent the requirement of reissuing dependant instructions. This, however, is not an inherency rejection, but an obviousness rejection. Applicant's solution would severely cripple out-of-order processing to a point that most efficiency derived from this several decade old technique would be lost. The technique of reissuing dependant instructions (including "the previous instruction") is overtly obvious to anyone skilled in the art and is doubtlessly "common, simple, fast, and effective" compared to Applicant's alternative solution.

Hughes Rejection

2. Applicant argues further about the limitation "generating an index", claiming that even if the definition given by Examiner in a previous office action is used, it is not found in the prior art.

Examiner disagrees. There does not appear to be any debate that the index value exists. Examiner is baffled at how Applicant believes that this value came into existence if not by being

"generated." Applicant is invited to explain why the conclusion is unreasonable that an existing value must be generated.

3. Applicant discusses the amendment to the independent claims requiring that the index value be fixed. Applicant believes that this amendment gets around the Hughes. Applicant states that in Hughes, "the entries in the LS2 buffer of Hughes are selectable based on the contents of the entry, (i.e., an index portion of the store address contained in the entry) which is clearly a variable value."

Examiner notes that paragraph 47 on of Applicant's specification states, "When the address associated with a load operation is received at 415, the load store unit may generate an index into the STLF buffer based on the address at 420." It is quite clear that Applicant's invention generates the index value from an address (quite similar to Hughes). Consequently, an vague and indefinite rejection has been added to this office action.

Examiner further points out that since Applicant has conceded that the index of Hughes is derived from the store address. Clearly, this falls under Examiner's definition of "generating" from the Office Action filed 28 November 2006, "taking the pre-existing bits and organizing them in a fashion that they can be utilized as an index."

4. Regarding claim 5, Hughes allocates memory using a "two way set associative structure" (page 16 lines 6-8). This satisfies the claim limitations of claim 5. Additionally, claim 8 fails to further limit claim 5 besides requiring that the additional index depend on the address "targeted by" the store operation, rather than "of" the store operation.

5. Regarding claim 6, Applicant's arguments are persuasive. The arguments with respect to claim 7 are rendered moot. This is additionally true with regards to Webb.

6. Applicant discusses the find-first algorithm of claim 10. Applicant states that, "the youngest of the operations may not be the first of the operations that correspond to a hit, and may not be selectable using a find-first algorithm."

Examiner asserts that it is unclear what weight to give the term "find-first algorithm." A search on Google Scholar brings up two hits for the term, including information about this outstanding application. Therefore, it is presumed that a "find-first algorithm" is an algorithm "to select a youngest issued store operation that is older than the load operation." A further discussion of "how" this is done is not required by the claim.

7. Regarding claim 11, Applicant's arguments are persuasive. This claim is more appropriately rejected as an obvious rejection. The same is true with regard to Webb.

8. Regarding claim 12, Examiner agrees with Applicant's arguments regarding inherency. The obviousness rejection discussed above still remains for reasons described above. Examiner notes that the use of "common art" is intended to be an Official Notice.

9. Regarding claim 4, Applicant asserts that the Official Notice taken on the data bus width does not adequately anticipate the limitations. In particular, Applicant states that instruction sets

of different processors may provide for store operations involving different number of bytes of data and/or the implementation of the instruction set may provide for different numbers of bus cycles for each store operation.

Examiner asserts that there is nothing within the reference to indicate the use of multi-clock memory operations. See page 25 line 30 to page 26 line 5. Additionally, even if there were multi-clock memory operations, it is still a reasonable interpretation to consider the operation of each separate clock cycle to be a separate operation. This argument is also applied to the rejection of claim 4 with respect to Webb.

Webb Rejection

10. Regarding claim 1, Applicant states that Webb describes forwarding data from the store data buffer 428 if the tag in store queue 426 and the tag reference match for the selected entry in the store queue 426. Applicant argues that this is different than what is required by claim 1.

Examiner disagrees. The STLF buffer is anticipated by the combination of buffer 428 and queue 426. The claim requires that "the plurality of entries" are included in the STLF buffer, which is satisfied by 428. Data is forwarded from "one of the plurality of entries" as described in col. 2 lines 8-15.

11. Regarding claim 5, Applicant states that Examiner's interpretation of the "additional index" is unsupported by the cited art.

Examiner disagrees. Claim 5 refers to allocating a store operation by generating an additional index that is dependent on a portion of the store address. This appears to be an indexing technique that is broad enough to fall under several techniques. This includes the "set associative" technique used in Webb (col. 4 line 58). The argument follows with respect to claim 8.

12. Regarding claim 6, Applicant's arguments are persuasive. The arguments with respect to claim 7 are rendered moot.

13. Regarding claim 9, Applicant asserts that the use of inherency is not proper. Applicant further asserts that Webb would not require operation verification if Webb was implemented "in such a way as to not forward an entry unless its correct selection is deterministic."

Examiner asserts that Applicant's proposed technique still requires a verification of the operation. If Webb chooses not to forward an entry unless it is correct, there must be some way to verify whether it is correct.

To further address Applicant's concern, an obvious rejection has been added to the Office Action.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the

state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RICHARD L. ELLIS
PRIMARY EXAMINER